



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,123	08/28/2001	Gurtej Singh Sandhu	303.676US3	6644

21186 7590 03/24/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
----------	--------------

2826

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. **09/941,123**Applicant(s) **SANDHU ET AL.**Examiner **Johannes P Mondt**Art Unit **2826**

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 46,47 and 57-82 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 46,47 and 60-82 is/are allowed.
- 6) ☒ Claim(s) 57-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/13/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/13/04 has been entered.

Information Disclosure Statement

The examiner has considered the items listed on the Information Disclosure Statement filed 2/13/04. A signed copy of Form PTO-1449 is enclosed with this Official Action.

Response to Amendment

Amendment filed 2/13/2004 together with the aforementioned Request for Continued Examination forms the basis of this Official Action. In said Amendment Applicant substantially amended claims 57, 58 and 59.

Response to Arguments

Although the amendment of claim 57 overcomes the rejection under 35 USC 112, however, prior art has been found with regard to the amended claims 57-59 as detailed below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. ***Claim 57*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Shankar et al (4,782,380) in view of Ikeda et al (5,239,196).

Shankar et al teach a semiconductor device such as inter alia a MOS transistor, comprising:

a layer of a titanium alloy (TiW) 40 (cf. col. 3, l. 47-58) formed overlying walls of a contact hole (for providing a contact between doped region 14 of said MOS transistor through an interconnect at 86; cf. Figures 1 and 3; col. 3, l. 27-36 and col. 6, l. 7-22); and

a titanium silicide contact (produced by annealing; cf. col. 4, l. 38-51: note the sputtered barrier layer referred to in line 39 is the barrier layer 40 discussed in col. 3, l. 47-58) having a composition that is different from the layer of titanium alloy, namely: titanium silicide, the contact being directly coupled to the layer.

Shankar et al do not necessarily teach the application of said MOS transistor in any specific sub-domain of interconnects for integrated circuitry (cf. col. 1, l. 8-13). In particular they do not necessarily teach the further limitations on memory array, control circuit and I/O circuit as claimed in claim 57.

However, it would have been obvious to include said further limitations in view of Ikeda et al. As shown by Ikeda et al, the integration into a memory device of a memory array (MAY; cf. Figure 2) with a control circuit CC operatively coupled to the memory array MB (said operative coupling is standard if not inherent for any useful control circuit to function) (cf. Figure 2 and column 29, lines 2-3) and an I/O circuit (cf. Figures 6 and 7), operatively coupled to the memory array (said operative coupling constitutes a standard application of MOS transistors (cf. title and abstract) is merely an obvious application of said MOS transistor (cf. column 60, lines 49-59), merely signifies an obvious application of said memory array. Furthermore, in order to exploit a memory array one has to integrate it with a control circuit for controlling the gate voltage, and exchange data with the memory array through input from and output to the outside, whence the I/O circuit of Ikeda et al.

Motivation to include said teaching by Ikeda et al into the invention by Shankar et al is therefore merely the exploitation of the standard manner in which a MOS transistor is exploited within integrated memory circuitry. *Combination* of said teaching with said invention is straightforward as the connections to and from, and the embedding of said MOS-transistor-comprising memory array into, the remaining circuitry does not depend on the specifics of the memory array. *Success* of the implementation of said combination can therefore be assured.

On claim 58: for lines 1-9 (all but final two lines) see discussion above of claim 57. Furthermore, with regard to the final two lines of this claim: said contact

hole in Shankar et al is filled with aluminum base metal 50 coupled to said titanium alloy layer 40 (cf. Figures 1 and 3; cf. col. 5, l. 5-23).

On claim 59: claim 59 only distinguishes from claim 57 through the final five (5) lines, which however only further limit the method of making, not the final structure. Therefore, the rejection of claim 57 applies verbatim to claim 59 as well.

Allowable Subject Matter

1. ***Claims 46-47 and 60-82*** are allowed:

Within the context of independent claims 46, 60, 72, 77 and 81 the (previously added) limitation that the contact be directly coupled to the layer of titanium alloy while the titanium alloy layer and titanium silicide layer must have different compositions (final lines of all independent claims in the above set of claims) is not taught by the cited art, nor rendered obvious through combination of the teachings of the cited art; nor did an update in the search yield prior art in this regard.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
March 20, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

